

What is claimed is:

1. A microcomputer that controls its operation clock signal in response to an external pulse signal including a header portion and a data portion with a format preset in the microcomputer,
5 said microcomputer comprising:

a reference data storage for prestoring a pulse length of the header portion and a pulse length of the data portion;

an external pulse signal capturing section for capturing the external pulse signal in synchronization with a low frequency
10 operation clock signal;

a comparator for comparing a header length of the external pulse signal with the pulse length of the header portion fed from said reference data storage, and for comparing a data length of the external pulse signal with the pulse length of the data
15 portion fed from said reference data storage;

a data storage for storing the data portion of the external pulse signal when the two comparisons by said comparator are each coincident; and

a clock switching section for decoding the data portion of
20 the external pulse signal stored in said data storage, and for switching the operation clock signal from the low frequency operation clock signal to a high frequency operation clock signal when the data portion decoded is a power-on instruction.

25 2. The microcomputer according to claim 1, wherein said clock switching section consists of software executed by a CPU.

3. The microcomputer according to claim 2, wherein
said external pulse signal capturing section comprises:
30 edge detecting means for detecting an edge of a pulse

of the input pulse signal by using an input of the external pulse signal as a trigger to start operation of said edge detecting means; and

clock switching signal output means for outputting,
5 when said edge detecting means detects the edge of the pulse of the input pulse signal, a control signal requesting said CPU to switch the operation clock signal, and wherein

said clock switching section halts generating all the operation clock signals when the external pulse signal is not
10 input for more than a predetermined time period in a power-off mode, and switches the operation clock signal in response to at least one of the control signal fed from said clock switching signal output means and the decoded result of the data stored in said data storage.

15 4. The microcomputer according to claim 1, wherein said external pulse signal capturing section, comprising multiple data storing means for storing data portions of a plurality of external pulse signals, successively transfers the data prestored in said data
20 storage to said multiple data storing means every time the external pulse signal is input, and wherein said clock switching section successively decodes the data portions stored in said multiple data storing means.

25 5. The microcomputer according to claim 1, wherein said reference data storage comprises: a header length register for prestoring a header pulse length of the header portion according to the format preset in the microcomputer; and a remote control data decision register prestoring a pulse length of the data
30 portion of the external pulse signal according to the format

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